

D-A101 126

ILLINOIS UNIV AT URBANA-CHAMPAIGN SOLID STATE ELECTRO-ETC F/G 20/12
SEMICONDUCTOR OXIDE INTERFACE STATES. (U)

MAY 81 C T SAH
SSELUI-TR-45

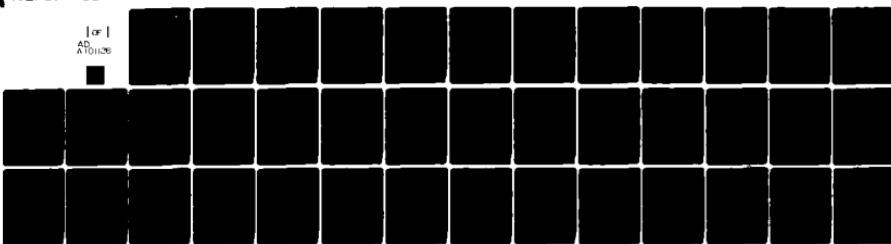
AFOSR-78-3714

AFOSR-TR-81-0546

ML

UNCLASSIFIED

1 of 1
AD 10126



END

DATE

FILED

7-4-81

DTIC

ADA101126

AFOSR-TR-81-0546

SEMICONDUCTOR OXIDE INTERFACE STATES

C.T. Sah

Solid State Electronics Laboratory
Department of Electrical Engineering
University of Illinois
Urbana, Illinois 61801

April 1981

LEVEL

DTIC

ELECTED

JUL 7 1981

Final Report
15 September 1978 to 28 February 1981

Grant Number: AFOSR-78-3714

Sponsored by: Department of the Air Force
Air Force Office of Scientific Research (AFSC)
Electronic and Solid State Sciences
Bolling Air Force Base
Washington, D.C. 20332

FILE COPY

Technical Monitor:

Dr. Jerry Silverman RADC/ESE
HANSCOM AFB, MA 01731

Approved for public release;
distribution unlimited.

DR

400-7-10

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER AFOSR-TR- 81 -0546	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) SEMICONDUCTOR OXIDE INTERFACE STATES	5. TYPE OF REPORT & PERIOD COVERED FINAL (15SEP78-28FEB81)	
7. AUTHOR(s) C. T. Sah	6. PERFORMING ORG. REPORT NUMBER SSELUI-TR-45	
9. PERFORMING ORGANIZATION NAME AND ADDRESS Department of Electrical Engineering University of Illinois Urbana, IL 61801	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 61102F 2306/B1	
11. CONTROLLING OFFICE NAME AND ADDRESS Air Force Office of Scientific Research/NE Electronic and Solid State Sciences Bolling Air Force Base, Washington DC 20332	12. REPORT DATE May 1981	
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	13. NUMBER OF PAGES 40	
16. DISTRIBUTION STATEMENT (of this Report)	15. SECURITY CLASS. (of this report) UNCLASSIFIED	
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)	15a. DECLASSIFICATION/ DOWNGRADING SCHEDULE	
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number)		
Silicon Silicon Oxide Surface States Oxide Charges Transient Capacitance Spectroscopy	Conductance-Voltage Characteristics Capacitance-Voltage Characteristics Photo-Current-Voltage Characteristics Metal-Oxide-Semiconductor	
20. ABSTRACT (Continue on reverse side if necessary and identify by block number)		
This final report gives a summary of the experimental and theoretical studies undertaken during the two-year AFOSR grant on the electrical properties and atomic origins of oxide charges and interface states in the silicon oxide-silicon MOS structure. Both UV light and KeV electron are used to probe these interface and oxide states. MOS C-V, G-V and photo I-V measurements are performed under computer control. Experiments have shown that trivalent silicon and nonbridging oxygen are likely to be the principal atomic defects that are responsible for the presence of the		

DD FORM 1 JAN 73 EDITION OF 1 NOV 55 IS OBSOLETE

UNCLASSIFIED

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

interface states and oxide charges. Hydroxyl or hydrogen ions can tie up these dangling bonds and neutralize these atomic defects but bonded H and OH can be readily released by the electrons or holes generated by the 10.2 eV photons or KeV electrons. After the defects are generated, they can be neutralized readily by exposing the MOS capacitor to forming gas (4% H₂ and 96% N₂) at 390°C for 10 minutes.

UNCLASSIFIED

-3- SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

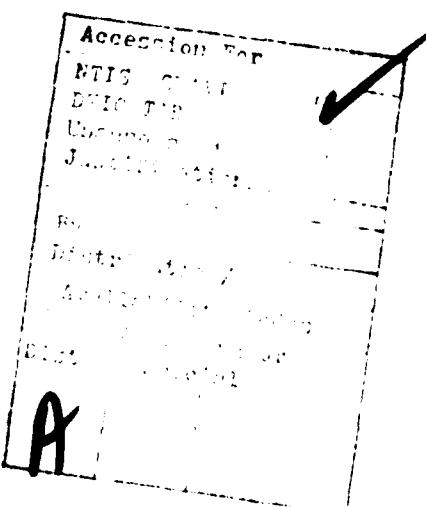
TABLE OF CONTENTS

Description	Page
TITLE PAGE	1
REPORT DOCUMENTATION PAGE	2
TABLE OF CONTENTS	4
LIST OF FIGURES	5
I. INTRODUCTION	6
II. RESEARCH OBJECTIVES AND STATEMENT OF WORK	10
III. STATUS OF RESEARCH EFFORT	11
3.1 INTERFACE STATES AND OXIDE CHARGES	11
3.1.1 Process Variations	13
3.1.2 Injection of Holes or Electrons into the Oxide by Vacuum Ultraviolet Light (VUV)	19
3.1.3 Generation of Holes and Electrons by KeV Electron Beam	30
IV. CUMULATIVE CHRONOLOGICAL LIST OF PUBLICATIONS	33
V. LIST OF PROFESSIONAL PERSONNEL	35
VI. INTERACTIONS (COUPLING ACTIVITIES)	37
6.1 CONTRACT SPONSORS	37
6.2 U.S. GOVERNMENT LABORATORIES	37
6.3 U.S. GOVERNMENT AGENCIES	37
6.4 U.S. GOVERNMENT AGENCIES	38
6.5 U.S. UNIVERSITIES	38
6.6 U.S. INDUSTRIES	38
6.7 FOREIGN GOVERNMENT - CHINA	38
6.8 FOREIGN GOVERNMENT - TAIWAN	39
6.9 FOREIGN VISITORS	39
6.10 U.S. PROFESSIONAL SOCIETY	39

LIST OF FIGURES

Figure	Page
1 The high frequency (1 MHz) capacitance-voltage curves at 297 and 77K of a silicon MOS capacitor before and after annealing in forming gas at 370°C for 30 minutes. B ₂₉₇ and B ₇₇ curves were taken before forming gas annealing and A ₂₉₇ and A ₇₇ were taken after annealing in forming gas.	14
2 The capacitance-voltage characteristics of a Al/SiO ₂ /Si MOS capacitor made on a radiation hard silicon oxide.	18
3 The one-MHz C-V curves of a radiation hard MOS capacitor after several photoinjections of holes. Curve 0 = original, Curves 1, 2, 3 and 4 = after each hole injection.	23
4 The C-V curves at 1 KHz and 1 MHz after VUV photoinjection of holes	24
5 The C-V curves after each electron photoinjection subsequent to the photoinjection of holes shown in Figure 3.	25
6 The one-MHz C-V curves at 100 and 302K before and after electron photoinjection without intermediate hole injections.	27
7 Effect of forming gas anneal of interface states. Interface state density versus energy. Curve 0 = initial device. Curve 8 = after hole injections followed by electron injections. Curve 9 = after annealing in forming gas at 390°C for 10 minutes.	29

AIR FORCE OFFICE OF SCIENTIFIC RESEARCH (AFSC)
 NOTICE OF TRANSMITTAL TO DDC
 This technical report has been reviewed and is
 approved for public release IAW AFR 190-12 (7b).
 Distribution is unlimited.
 A. D. BLOSE
 Technical Information Officer



I. INTRODUCTION

The dimension of semiconductor devices (diodes and transistors) in the current state-of-the-art and future generations of integrated circuit is continually decreasing to achieve high component and function densities and performance. Fundamental semiconductor effects, not important previously in large area transistors and large integrated circuits, are becoming increasingly important in these microstructure devices. For example, in the current high density silicon memory chip with a memory cell area of $400 \mu\text{m}^2$, there are about 10^6 signal electrons under the gate of the MOSFET (metal-oxide-semiconductor field-effect transistor). The number of signal electrons would decrease by a few orders of magnitude if the device dimension is further reduced in future MOSFETs with submicron dimensions. When the number of signal electrons is very small, all types of statistical fluctuations will become important since they generate a significant amount of noise to create soft errors or to produce a large number of defective transistors to render the integrated circuit inoperative. For instance, randomly distributed trapped charges in the gate oxide and at the interface are normally present in a MOSFET. They are introduced during the device fabrication processes such as high temperature oxidation and diffusion, chemical vapor deposition, ion implantation, ion and plasma etching, and electron-beam or x-ray lithography. Although they are present in low concentration, they can become serious fundamental limitations on the reproducibility and yield of a very high density integrated circuit composed of submicron MOSFETs because the number of these trapped charges at a given MOSFET gate can become comparable or even exceed the number of signal electrons when the dimension of the MOSFET is very small.

The importance of the statistical fluctuation of the defect and impurity concentrations in the semiconductor bulk on the characteristics of submicron

bipolar integrated circuits is also obvious from the above description for the MOSFET integrated circuit. When the number of signal electrons in each bipolar transistor diminishes as its dimension decreases, the statistical fluctuations can short-circuit the transistor or drastically alter its characteristics and degrade its performance.

In addition to the statistical fluctuations of oxide, interface and bulk defects and impurities, the device theory and the device model must also be extended or revised in order to accurately characterize very small devices. Fundamental understanding of the atomic nature of these imperfections is needed to better control their concentration. Mathematical theories are needed to provide more accurate device models which are sufficiently accurate and simple to be usable in CAD (computer-aided-design) of very large scale integrated circuits.

When the dimensions of a transistor shrink, two- and three-dimensional effects become increasingly important. The one-dimensional MOS transistor theory, which has been used successfully to design small, medium and even moderately large scale silicon integrated circuits, is no longer adequate. For example, the current state-of-the-art silicon integrated circuits already uses MOSFET of a few micron dimension which is so small that its gate threshold voltage is strongly influenced by the length as well as the width of the gate electrode, making it essential to use a three-dimensional device model. As another example, the very high speed GaAs, InP or Si junction-gate field-effect transistor, MESFET (metal-semiconductor field-effect transistor), employs such a short and narrow Schottky barrier gate to control the source to drain current and to achieve high speed that not only the aforementioned two- and three-dimensional effects are important but the basic phenomenon of electron transport in the semiconductor conduction channel is also drastically altered.

from the classical phenomenon of diffusion and drift governed by the Boltzmann equation. As the gate length is shortened while the source-to-drain d.c. operating voltage is maintained at 5 Volts, the longitudinal electric field in the channel becomes very high and the high electric field effects must be included in the Boltzmann equation. As the channel is reduced further and the electric field increases further, the Boltzmann equation must be replaced by a ballistic transport equation for electrons with infrequent scattering by impurities, phonons and the boundary surfaces enclosing the conduction channel.

This final report describes a study on some of these problems which are relevant to the fabrication, characterization and operation of future submicron integrate circuit transistors. It describes the effort and the research status of the final two years of three consecutive grants with no future grant renewal to be anticipated. This final two-year effort was a continuation of two previous grants, AFOSR-71-2067 (September 15, 1971 to September 14, 1975) and AFOSR-76-2911 (September 15, 1975 to September 14, 1978). The current grant, AFOSR-78-3714 covers the period of September 15, 1978 to September 14, 1980 with a no-added-cost-extension to April 28, 1981.

A major effort was initiated during the second of the previous two grants (AFOSR-76-2911) to upgrade as well as to design and construct several unique and sophisticated equipment setups since they are very critically needed in the detailed electrical characterization of the defect and impurity centers in the oxide, at the interface as well as in the semiconductor bulk. These included (1) a 10.2 eV vacuum ultraviolet light source which allows in-situ measurements of MOS characteristics after each irradiation in vacuum from 77K and up, (2) a 0-15 KeV electron source in a vacuum chamber which also allows in-situ measurements of MOS characteristics after each irradiation at 300K, (3) a photocurrent-voltage measurement setup in room ambient for MOS

capacitors at 300K to determine the spatial distribution of the oxide charges using a monochromatic light source from 2 eV to about 6 eV and (4) several liquid nitrogen and liquid helium temperature capacitance transient spectrometer to characterize deep and shallow levels at the surface and in the bulk. All of these equipments have been put into operation under the real-time control of two linked minicomputer systems (Hewlett-Packard Model 1000M and 1000F) and a desk computer (Hewlett-Packard Model 9845T) to facilitate accurate data acquisition and analysis. This effort of setting up the unique and sophisticated equipment has extended into the first year of the current grant period and is largely completed. The equipment has been operational during the final or the second year of the current grant.

The research objectives are described in section II and the status of the research effort is given in section III. A cummulative chronological list of publication is given in section IV. Professional personnel associated with the research efforts is listed in section V. Interaction with other active workers are briefly summarized in section VI. Specific applications of the results and findings from this research effort are obvious from the various introductory discussions and justifications of specific studies made in section III where the status of the research effort is given, and thus, they are not repeated in a separate section as suggested by the guideline.

During the two year grant, three M.S. and one Ph. D. theses in Electrical Engineering and one Ph. D. thesis in Physics were completed. Eleven papers have been published in engineering and scientific journals and one is being published either in April or May of 1981. One junior faculty member and nine graduate students participated in this research. One of the graduate students remained for three years as a faculty member who was instrumental in setting up the computer automated data acquisition system.

II. RESEARCH OBJECTIVES AND STATEMENT OF WORK

The objective of this research is to determine the properties and atomic origin of oxide traps and interface states on a semiconductor surface covered with an oxide, specifically the thermally oxidized silicon. The approach focuses on detailed experimental and theoretical characterizations of these imperfections by means of unique experimental techniques, such as the photocurrent-voltage method; the capacitance- and conductance-voltage method with temperature and signal frequency as the parameters; the capacitance transient spectroscopic methods, including voltage-stimulated capacitance transient (VSCT), voltage-stimulated capacitance transient spectroscopy (VSCTS also known as DLTS); and the current transient methods, including the dark current transient (DCT), the photon beam induced current transient (PBIC), and the electron beam induced current transient (EBIC). The generation, annealing, regeneration, and migration of these imperfections are controlled by fabrication conditions (oxidation temperature, time, ambient, cooling rate) and post fabrication exposure to a 10.2 eV ultraviolet light source or a 0-15 KeV electron beam.

III. STATUS OF RESEARCH EFFORT

The status of the research projects supported by this grant is reported in this section. The measurement equipment has been assembled or built and successfully operated. Results using this equipment setup are described. A number of research projects were completed, resulting in M.S. or Ph.D. theses in electrical engineering or in physics and the publication of articles in technical journals. There are also a number of projects which had just begun using this equipment. They involve more comprehensive experiments and require considerably more time and several future Ph.D. theses to complete, but their completion cannot be assured due to the discontinuation of grant supports in silicon material and silicon device areas from this DOD research office (AFOSR). Description of the completed projects and the incomplete projects are given in the following subsections. The presentation is grouped according to the main generation and annealing methods for oxide traps and interface states.

3.1 INTERFACE STATES AND OXIDE CHARGES

The main purpose of this project is to explore the atomic origin as well as to characterize the electronic and optical properties of the localized electronic states at the insulator-semiconductor interface (known as interface or surface states) and in the oxide (known as the oxide charges or oxide traps). The reliability and the electrical properties of almost all the semiconductor devices are critically dependent on the generation, annealing and diffusion of these localized states. In spite of nearly twenty years of studies and many successful applications of the SiO_2 -Si MOS

system,¹ much of the fundamental mechanisms and atomic make-up of the defects in this system are still poorly understood.² Attempts have been made to construct atomic models based on past observations and recently designed experiments.³ However, many experiments are still needed to delineate the models and to understand the effects of the many parameters on the electrical stability of the SiO_2 -Si system. Such a detailed understanding is crucial for further advancing the technology to produce solid state electronic device structures of microscopic scale for very Large scale (VLSI) and very high performance (VHSIC) integrated circuits whose device and function densities approach that of molecular or atomic densities.

The origin of the interface states and oxide charges on oxidized silicon and their electronic and physical-chemical properties are investigated by three methods: (i) variation of process parameters, such as temperature and ambient of oxidation and post-oxidation heat treatment, (ii) generation of electrons and holes at the oxide surface by ultraviolet light (photon energy greater than about 8 eV since the energy gap of SiO_2

¹The first serious attempt to use thermally grown oxide to improve the properties of silicon diodes and transistors was described by workers at Bell Telephone Laboratories in 1959: See M. M. Atalla, E. Tannenbaum and E.J. Scheibner, "Stabilization of silicon surfaces by thermally grown oxides," Bell System Technical Journal, 38, 759-783, May 1959.

²B.E. Deal, "The current understanding of charges in the thermally oxidized silicon structure," J. Electrochemical Soc., 121, 189C-205C, June 1974; and *Semiconductor Silicon*, Proceedings of the Third International Symposium of Silicon Materials Science and Technology (May 3-13, 1977), published by the Electrochemical Society, Princeton, NJ.

³C.T. Sah, "Origins of interface state and oxide charges generated by ionizing radiation in thermally oxidized silicon," Invited paper given at the 1976 IEEE Annual Nuclear Science Symposium, IEEE Transactions on Nuclear Science, NS-23, No. 6, 1563-1568, December 1976.

is about 8 eV) and subsequent transport through the oxide layer and trapping at oxide traps and interface states, and (iii) generation of interface states as well as oxide charges by KeV electron irradiation. The oxide charge and the interface state densities are obtained by MOS capacitance- and conductance-voltage measurements over a wide range of temperature (4-300K) and signal frequency (1 to 10^8 Hz). The centroid locations of the oxide charge distribution are determined by the d. c. photocurrent-voltage characteristics. Transient photocurrent measurements during ultraviolet-light and KeV electron excitation are also made to determine the charge transport property in the oxide and recombination properties of the interface states.

3.1.1 Process Variations

Many experiments have been performed during the grant period to determine the effect of temperature and ambient of oxidation and post-oxidation heat treatment on the properties of oxide charges and interface states. Most of these experiments are initial sets of experiments to get some preliminary data so that further experiments can be designed to test the various models of the atomic origin of oxide charges and interface states.³

One of the earlier experiments was a simple one in which a completed MOS capacitor is heated in forming gas (4% H₂ and 96% N₂) at 370°C in a die bonding station. The annealing of the interface states and oxide charges by the forming gas or hydrogen is indicated by the high-frequency C-V curves at 297 and 77K shown in Figure 1. The curves labeled B₇₇ and B₂₉₇ are those taken before the heat treatment in forming gas while those labeled A₇₇ and A₂₉₇ are those taken after heat treatment in the forming gas. The large distortion or change in shape of the C-V curves before forming gas

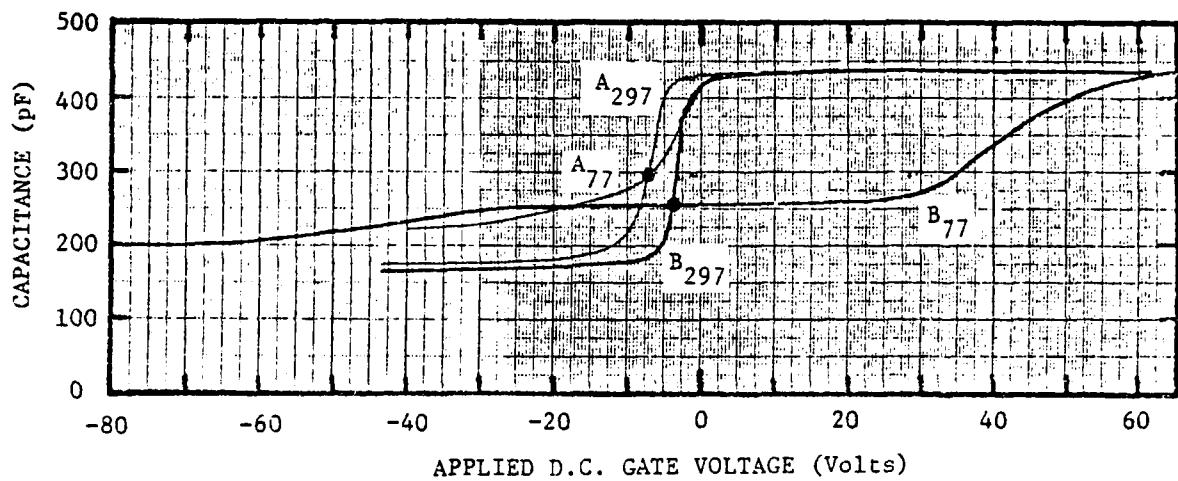


Figure 1 The high frequency (1 MHz) capacitance-voltage curves at 297 and 77K of a silicon MOS capacitor before (curves B₇₇ and B₂₉₇) and after (A₇₇ and A₂₉₇) annealing in forming gas at 370°C for 30 minutes.

annealing indicated by curves B_{297} and B_{77} reflects an extremely high density of interface states near the band edges. The positive voltage shift is more than 40 volts which gives an interface state density of about 4×10^{12} states/cm² near the conduction band edge which is calculated from the voltage shift and the oxide thickness of about 2700A. These states are acceptor-like due to the voltage shift in the positive direction from 297 to 77K. The negative voltage shift below the cross over point has two plateaus. The lower plateau has not dropped to the final value even at -90 volts. Thus, the donor-like interface states near the valence band have a density higher than 8×10^{12} states/cm².

The C-V curves after annealing in the forming gas, A_{297} and A_{77} , show a substantial reduction of interface states and a slight increase of positive oxide charges. The reduction of the interface states is deduced from the voltage differences between A_{297} and the A_{77} C-V curves both above and below the cross-over point which are smaller than the differences between B_{297} and B_{77} curves taken prior to forming gas anneal. The difference above the cross-over point is less than 5 Volts, indicating that the forming gas annealing process has reduced the interface states in the upper half of the band gap by a factor of 10 or more (5 Volts versus 40 to 50 Volts given by curves B_{77} and B_{297}). The difference below the cross-over point is about 10 to 20 Volts, indicating that there are still about 10^{12} donor-like states/cm² at the interface which are not annealed out by heating in the forming gas.

The slight increase of the positive oxide charges is suggested by the negative voltage shift of the A_{297} curve from the B_{297} curve. They look almost parallel and the horizontal shift is less than 5 Volts. This translates to an increase of oxide charge of about 4×10^{11} q/cm².

These experiments are consistent with our trivalent silicon model of interface states.³ Initially, there is a high density of dangling silicon bonds at the interface as indicated by the voltage shift between the B₂₉₇ and B₇₇ C-V curves. These states were generated during heating in the inert Argon ambient after thermal oxidation. These dangling bonds are tied up by hydrogen and/or OH⁻ ions during the annealing step in the forming gas ambient. This tie-up of the dangling silicon bonds substantially reduces the magnitude of the random atomic potentials at the interface which had perturbed the band states into the energy gap. The annealing process apparently also introduced some positive charges in the oxide whose origin is not known at present but could conceivably be due to sodium ions present on the sample surface during processing.

Photocurrent-Voltage measurements on the sample before forming gas anneal show that most of the oxide charges are located within 50-100A of the oxide-silicon interface.

Measurements have also been made on MOS capacitors with radiation-hard silicon dioxide. Radiation sensitivity will be discussed in the following subsections. The 700A oxide was grown in ultra high purity (UHP) oxygen through a cold trap. The oxidation was terminated by a fast pull from the furnace and cooled in the UHP oxygen ambient in about 5 minutes to room temperature. This oxide was protected by a 10000A thick aluminum for an extended period (about five years since it was fabricated in 1975 by a DOD contractor). The thick aluminum was then etched off in our university laboratory and a thin aluminum layer (150A) was then evaporated onto the sample, and a 70 mil diameter aluminum gate was defined by photolithography. Our processing did not contaminate the

oxide and preserved its low sodium ion drift and low oxide charge and interface state density properties.

These samples show very low density of interface states as revealed by the frequency dependences of the capacitance-voltage curve in Figure 2. The two C-V curves are taken at 10^3 and 10^6 Hz. Their coincidence indicates essentially no interface states. The slight separation of the two curves in the knee region is due to the presence of a bulk contamination (probably gold) during oxidation at the industrial laboratory rather than to interface states. Its presence was also detected in measurements made in 1975 immediately after part of the samples were oxidized and converted to MOS capacitors. The main feature of this oxide is its low to medium oxide charge density as revealed by the -2 Volts flat band voltage of the C-V curve and the extremely low density of interface states just discussed. It demonstrates that (1) oxide charge density and interface state density are not necessarily proportional, as some of our 10-year-old experiments and some recent experiments by others indicate, (2) the oxide charge in this case may be due to an excess oxygen species, such as the nonbridging oxygen proposed in our review³ and suggested by the experiments of Stivers performed under this grant and described in the next subsection, which has a large residual density in the oxide during the fast cool at the end of oxidation in the oxygen ambient, and (3) the low interface density arises from the lack of silicon dangling bonds, trivalent silicon or an oxygen deficient layer at the oxide-silicon interface, again due to the fast cool in the oxygen ambient. These results and interpretations are again consistent with the proposed models of oxide charges and interface states in our review paper.³

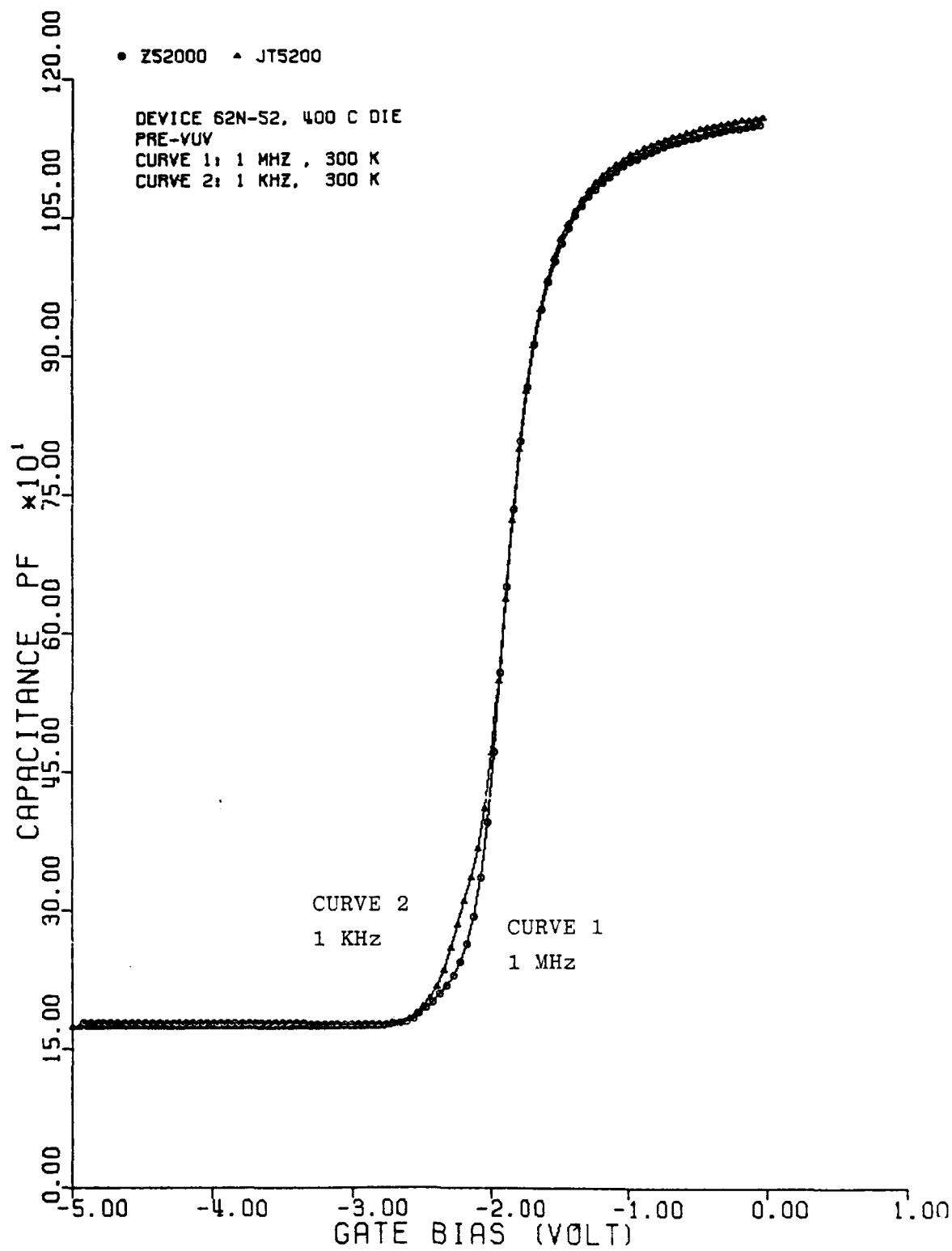


Figure 2 The capacitance-voltage characteristics of a Al/SiO₂/Si MOS capacitor made on a radiation hard silicon oxide.

3.1.2 Injection of Holes or Electrons into the Oxide by Vacuum Ultraviolet Light (VUV)

The atomic nature of the oxide traps and interface states can be further probed by measurements of the capture rates of the electrons or holes photo-injected into the oxide and by measurements of the change of trap densities during and subsequent to each photo-injection process. The energy gap of SiO_2 is about 8 eV. Thus, to photo-inject electrons or holes into the oxide, a light source of more than 8 eV energy is required. A vacuum ultra-violet (VUV) monochromatic light source is built which has a liquid nitrogen dewar at the exit slid to hold an MOS sample for measurements over the 77-300°K temperature range. The vacuum is produced by an ion pump and is needed to eliminate atmospheric absorption of the UV light. The UV light is provided by the Lyman alpha line (10.2 eV) of a hydrogen discharge lamp. The VUV photons are directed at the thin aluminum gate (150A) of the MOS capacitor. It is mostly absorbed in a thin surface oxide layer beneath the aluminum gate due to the very high absorption coefficient of the SiO_2 . Electron-hole pairs are generated at this surface layer of the oxide. If a positive d.c. voltage is applied to the aluminum gate during exposure to the UV light, the photo-generated holes are injected into the oxide from the oxide surface. If a negative d.c. voltage is applied during the exposure to the VUV light, electrons are injected into the oxide from the oxide surface. The injected holes or electrons will drift and diffuse through the oxide and some will be captured by the oxide traps to charge up the neutral oxide traps or to neutralize the charged oxide traps. The change of the trapped charge density is monitored by the shift of the high frequency capacitance-voltage (C-V) curve of the MOS capacitor.

From the rate of change of the voltage shift of the C-V curve, the electron and hole capture rates can be determined. From the shift of the voltage magnitude of the C-V curves, the trapped charge concentration can also be determined. From the distortion of the C-V curve, the interface state density can be determined. Finally, a photocurrent-voltage measurement using photons of 3-5 eV to excite electrons over the Al-SiO₂ barrier or the SiO₂-Si barrier will give the location or the centroid of the oxide charge distribution. Thus, a wealth of information can be obtained on the properties of the oxide traps and interface states, and this information can provide clues on the atomic nature of these imperfection centers.

An extensive study on the nature of the oxide traps has been made by Alan R. Stivers who reported his findings in his doctoral thesis in physics⁴ and in a journal article.⁵ The VUV as well as the photocurrent-voltage systems were designed and built by Stivers. They are described in his thesis⁴ and paper.⁵

Since detailed descriptions of the results are given in these publications, only a summary is given here.

The oxides used in these experiments were grown under temperature and cooling ambient conditions to produce high densities of interface states and oxide traps so that we would not be hindered by noise and accuracy when these densities are extremely low. However, due to the high

⁴ Alan R. Stivers, "Oxide charge traps and interface states at the Silicon-Silicon dioxide interface," Ph.D. thesis in Physics, University of Illinois, June 1979. Available through University Microfilm, Inc. Ann Arbor, Michigan.

⁵ A.R. Stivers and C.T. Sah, "A study of oxide traps and interface states of the silicon-silicon dioxide interface," Journal of Applied Physics, 51, 6292-6304, December 1980.

densities, some fine features, such as interface density peaks, are masked. Measurements on industrial silicon oxides which have low densities of interface state and oxide trap densities have also been made, subsequent to Stivers' work. These will be described after summarizing Stivers' results on high oxide-charge-density oxides.

The main conclusions of Stivers' experiments on the oxide traps are:

- (1) There are two donor-like neutral hole traps with hole capture cross sections of 6×10^{-14} and $1 \times 10^{-15} \text{ cm}^2$.
- (2) Both of these donor-like traps are efficient electron traps with an electron capture cross section of $3 \times 10^{-13} \text{ cm}^2$.
- (3) An acceptor-like electron trap is also detected with the electron capture cross section of $1 \times 10^{-15} \text{ cm}^2$. It anneals out at 800°C in dry oxygen.
- (4) Annealing kinetics suggest that the larger donor-like hole trap is an excess silicon center (trivalent silicon) and the smaller donor-like hole trap is an excess oxygen center (nonbridging oxygen).
- (5) Photo I-V measurements indicate that these traps are located within 50A of the oxide-silicon interface.

Another series of experiments is performed using the VUV injection method to determine the nature of the interface states in which radiation-hard MOS capacitors described in the preceding section (3.1.1) were used. The initial interface state density is very low as revealed by the 1 KHz and 1 MHz C-V curves shown in Figure 2.

Many high-frequency (1 MHz) C-V curves were taken during VUV hole injection and some of these are shown in Fig. 3 where the numerical curve labels indicate increasing number of holes injected. Curve 0 is that of the original sample prior to irradiation. Note the large distortion of the C-V curves with each increasing hole injection, indicating the generation of interface states. To be sure that these distortions are not due to inhomogeneous VUV light illumination, 1 KHz and 1 MHz C-V curves are also compared at the end of illumination. These two C-V curves are shown in Figure 4. The large frequency dependence of the C-V curve during VUV light irradiation proves that interface states are generated.

One may note that the C-V shift along the voltage axis is small (~ 1 V or $3 \times 10^{11} \text{ cm}^{-2} \text{ v}$) for these radiation-hard oxides compared with those whose initial oxide trap density is high (~ 60 V or $4 \times 10^{12} \text{ traps/cm}^2$).

After the above hole injection, the d.c. voltage applied to the aluminum gate is reversed to a negative value of -15 V to cause electron injection into the oxide. The 1 MHz C-V curves are shown in Fig. 5 whose numerical labels (5,6,7,8,9) correspond to increasing electron injection. Even after electron injection for a long time, the one-MHZ C-V curve (such as Curve 8) does not return to its original position before hole injection (Curve 0 in Fig. 3). Curve 9 nearly coincides with Curve 0 and it was taken after annealing the MOS capacitor in forming gas at 390°C. This annealing experiment is discussed later.

These results on radiation hard silicon dioxide show that

- (1) interface states are generated by capture of photo injected holes and
- (2) interface states generated by hole injection and capture cannot be eliminated completely by electron injection and electron capture.

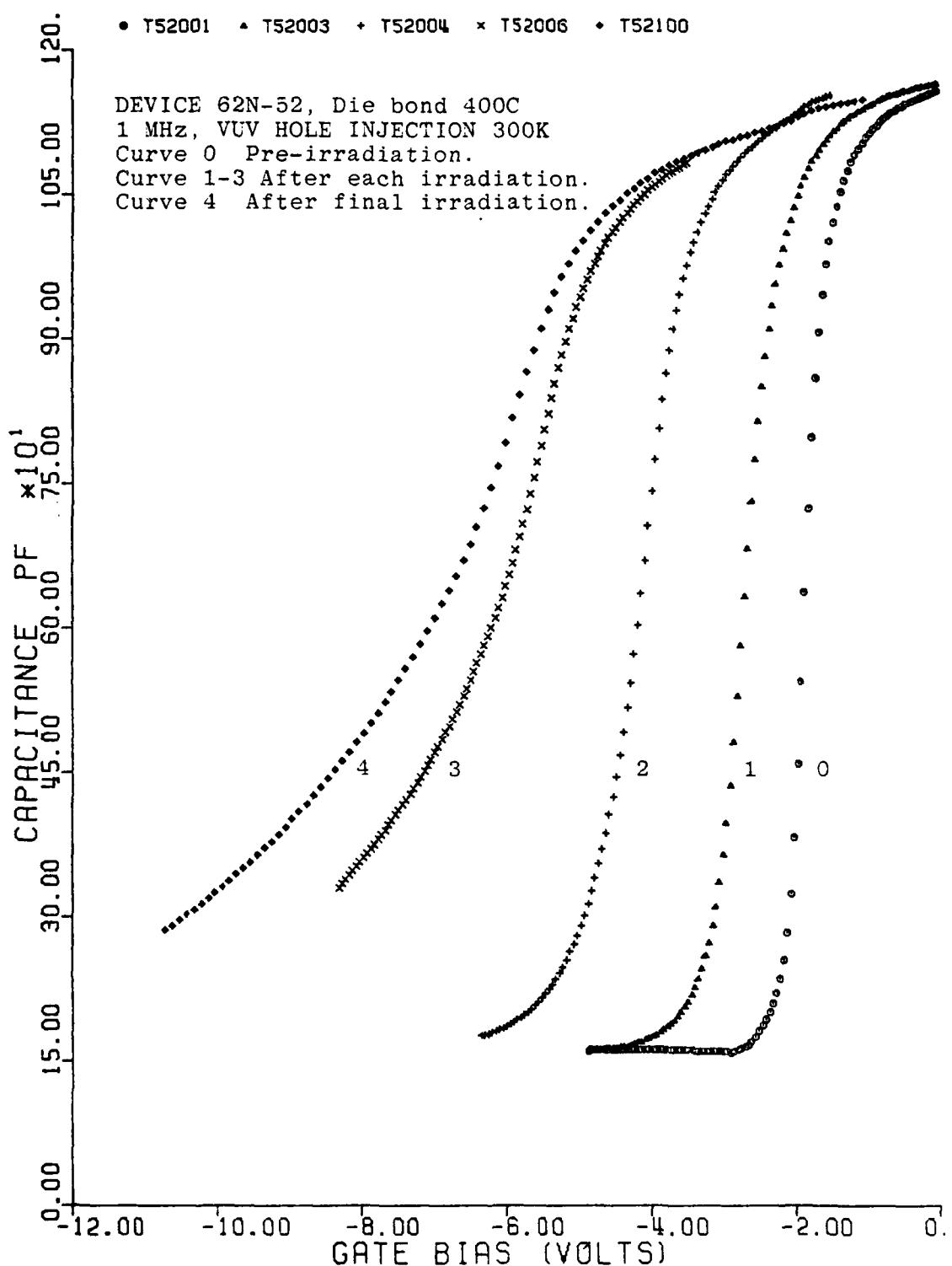


Figure 3 The one-MHz C-V curves of a radiation hard MOS capacitor after several photoinjections of holes. Curve 0 = original, Curves 1, 2, 3 and 4 = after each hole injection.

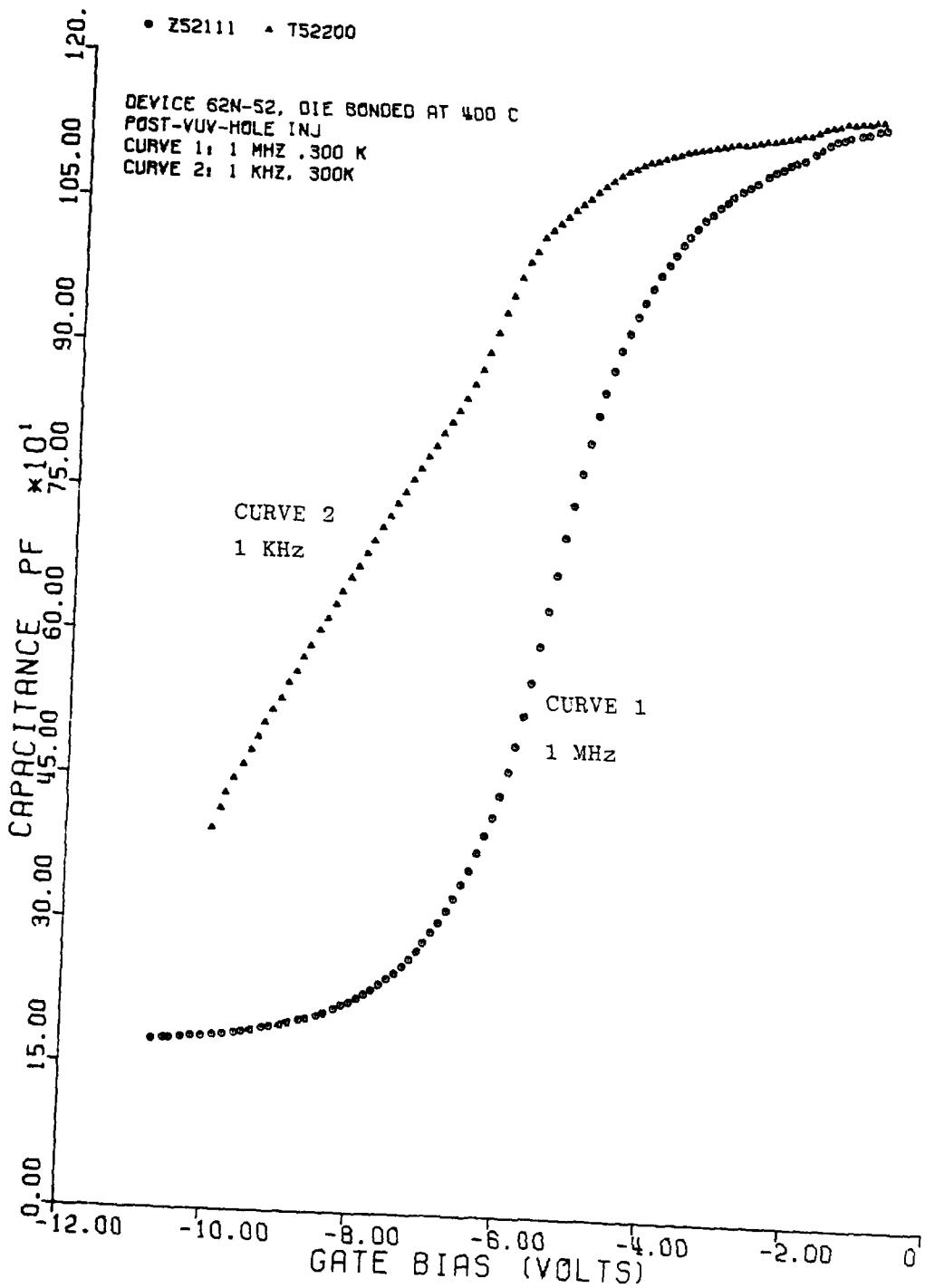


Figure 4 The C-V curves at 1 KHz and 1 MHz are VUV photoinjection of holes.

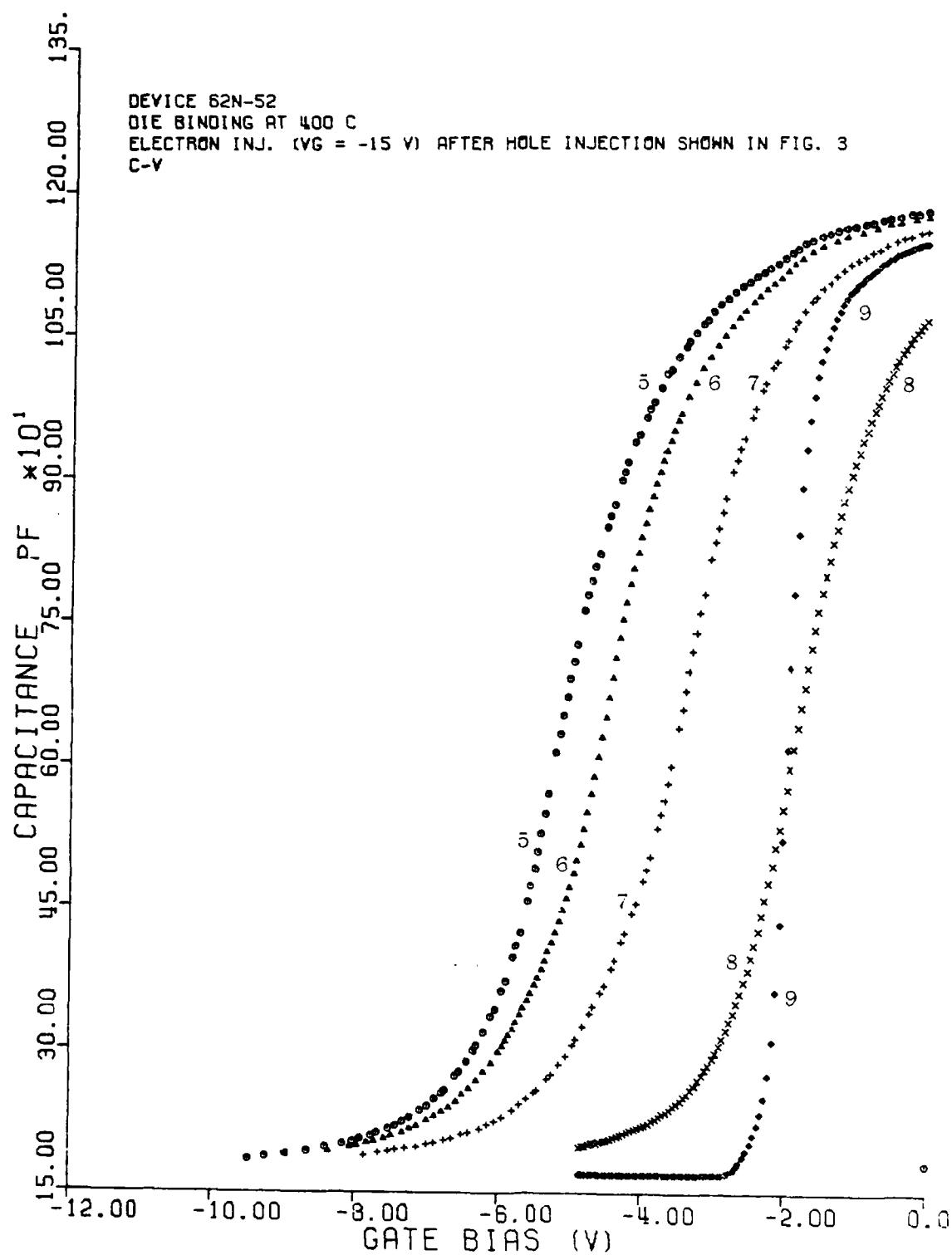


Figure 5 The C-V curves after each electron photoinjection subsequent to the photoinjection of holes shown in Figure 3.

These results leave us with only one plausible atomic model which had been proposed earlier based on fundamental reasoning,³ that is, the interface states generated must involve (1) breaking the Si-OH or Si-H or or weak Si-Si bonds and (2) a physical displacement of H, OH or Si from its former site. The impurity models involving H or OH is favored due to annealing of the interface states in forming gas which contains hydrogen, to be described below.

The physical displacement of an atomic species is the fundamental requirement of the above model for interface state generation. This was emphasized in our review paper³ and further demonstrated by these current experimental results. The generation of the interface states by hole capture is not 100% reversible by electron capture as observed in these experiments. This can only be explained by a bond breaking and atomic displacement model.

A further demonstration of these two atomic properties of the interface states is given by the VUV electron injection experiment. The C-V curves taken before electron injection at 302K and 100K (curves 1 and 2) and after electron injection (curves 3 and 4) are given in Fig. 6. They show that initially there is little or no interface states since curves 1 and 2 are nearly identical to the ideal theoretical C-V curves at these two temperatures, 302K and 100K. However, after electron injection, there is a very large difference between the 100K and 302K C-V curves (curves 3 and 4 in Fig. 6) which indicates the presence of a high density of interface states. This shows that a high density of interface states is also generated by electron injection and capture alone without a previous hole injection experiment.

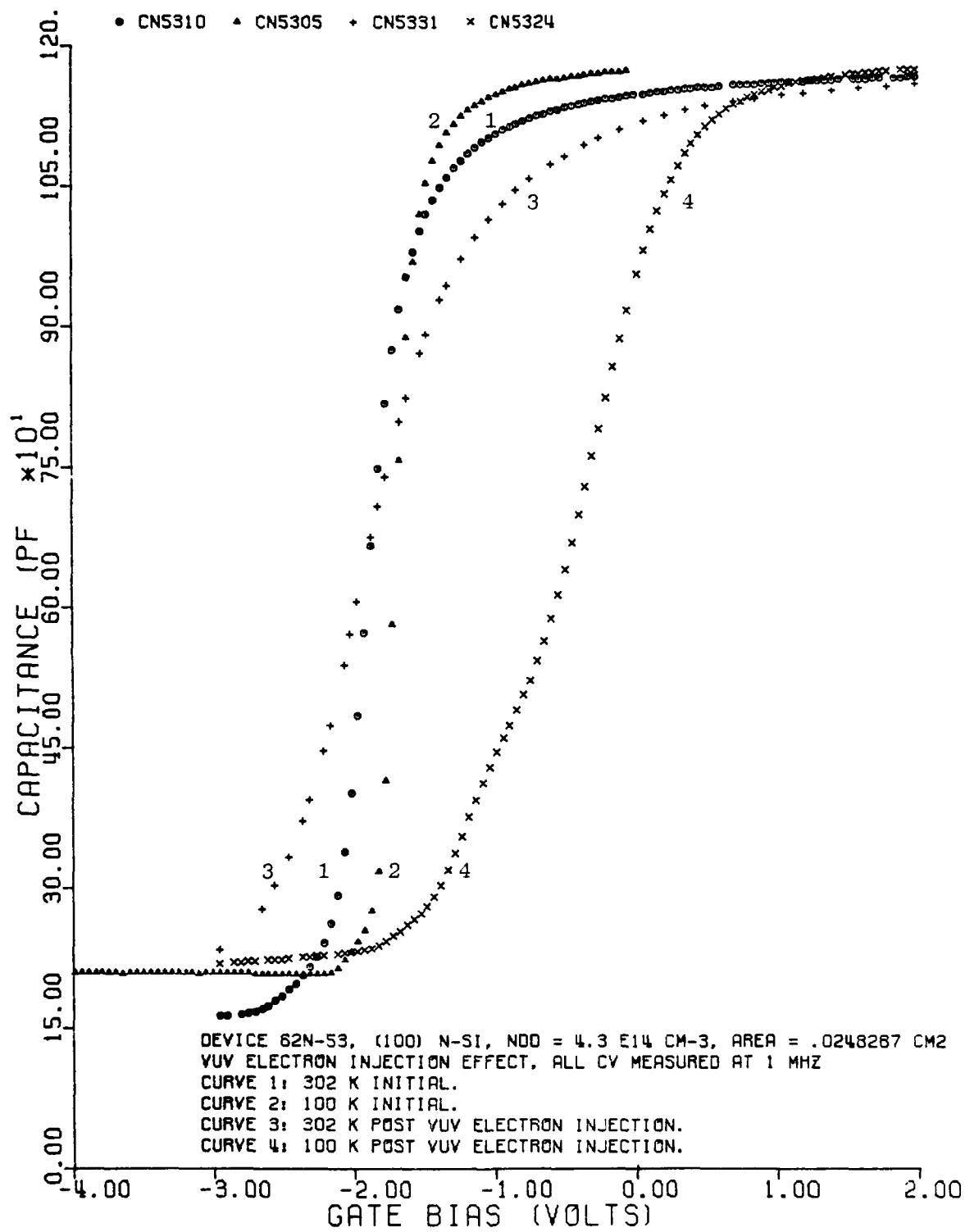


Figure 6 The one-MHz C-V curves at 100 and 302K before and after electron photoinjection without intermediate hole injections.

These results are in contrast with the earlier results of Stivers (references 4 and 5 on p.15) who observed little increase of interface states during hole or electron injection. The difference is that Stivers' oxide has very high initial density of interface and oxide trap states and they mask the additional interface states generated during electron or hole injection. On the other hand, the current experiments are performed on radiation hard oxides which have low densities of interface states and oxide traps or low densities of trivalent silicon dangling bonds and non-bridging oxygen dangling bonds so that small increases of interface states can be detected readily.

Another experiment was performed to show that the interface states generated by hole and electron injections can be completely annealed out by exposure of the MOS capacitor to a hydrogen containing ambient at a moderately high temperature. The MOS capacitor, whose C-V curve is given by Curve 3 in Fig. 5 after hole and electron photo-injection, was heated at 390°C for 10 minutes with zero applied gate voltage in forming gas (4% H₂ and 96% N₂). The C-V curve after annealing is Curve 9 in Fig. 5, which almost coincides with the original C-V curve prior to hole and electron photo-injections given by Curve 0 in Fig. 3.

The annealing by forming gas is so complete that a Terman's analysis of the interface state density is made to determine if any interface states still remain after forming gas anneal since the C-V curves 0 and 9 essentially coincides. The density of state curves of the interface states based on the Terman method are shown in Fig. 7 for the three conditions: (i) prior to hole injection (C-V curve 0 in Fig. 3), (ii) after electron injection (C-V curve 8 in Fig. 5) and (iii) after forming

VUV IRRADIATION AND F.G. ANNEAL EFFECT
 DEVICE 62N-52, 400 C DIE BONDED IN N2.
 $T = 297 \text{ K}$, $\text{COX} = 1192.1 \text{ PF}$, $\text{NDO} = 4.37 \text{ E14 CM}^{-3}$, $\text{AREA} = .0246287 \text{ CM}^2$
 INITIAL $\text{VFB} = -1.889 \text{ V}$, POST-VUV \pm INJ $\text{VFB} = -1.86 \text{ V}$, POST F.G. $\text{VFB} = -1.97 \text{ V}$
 DENSITY OF INTERFACE STATE VS ENERGY (LOG 10)

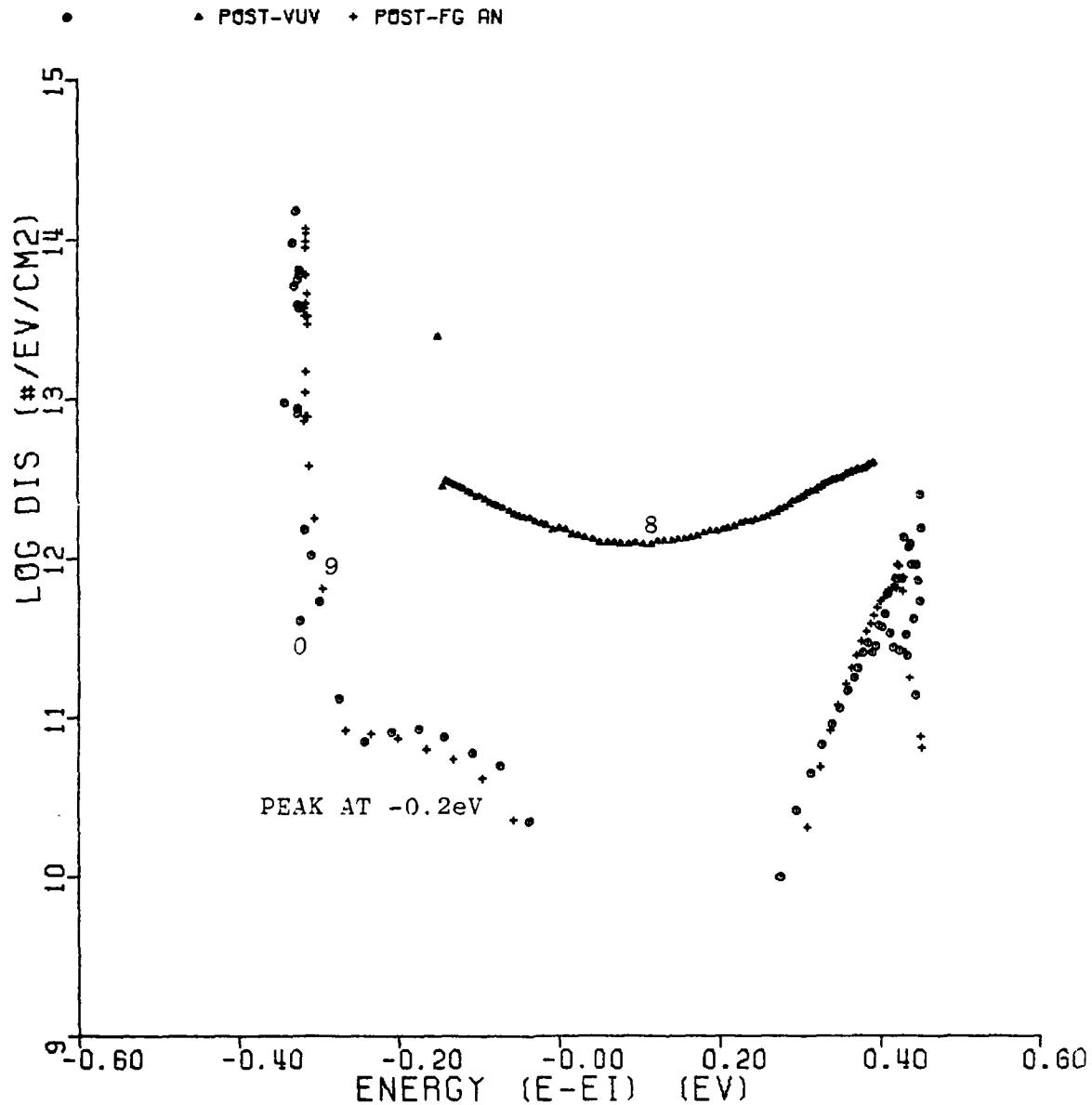


Figure 7 Effect of forming gas anneal of interface states. Interface state density versus energy. Curve 0 = initial device. Curve 8 = after hole injections followed by electron injections. Curve 9 = after annealing in forming gas at 390°C for 10 minutes.

gas annealing (C-V curve 9 in Fig. 5). Note the large remaining interface state density of nearly 10^{12} states/cm²-V given by the partial-U-shaped curve (Curve 8) after electron injection. This further shows that electron injection does not remove all of the interface states generated by hole injection, a conclusion we had reached already in our preceding discussions.

However, the density of state curves 0 and 9 are essentially identical, indicating all the interface states generated by hole and electron injections are annealed out at 390°C in 10 minutes of forming gas. Note also that there is a small interface density peak at about 0.2 eV below the silicon midgap in Fig. 7. This peak is small, about 10^{11} states/cm²-V, and is masked in our earlier experiments reported by Stivers whose samples had a very high interface state density (about 10^{13} states/cm²-V).

The mechanisms of interface state annealing have been studied further by varying the ambient composition and annealing temperature and time. Only preliminary results have been obtained thus far.

3.1.3 Generation of Holes and Electrons by KeV Electron Beam

The nature of the oxide traps and interface states can be further studied using a KeV electron beam to generate electrons and holes. The difference between this method of electron-hole pair generation and the method using 10.2 eV light described in the previous section is that here the electron-hole pairs are generated fairly uniformly in the entire silicon dioxide rather than only in a thin oxide layer beneath the aluminum by the 10.2 eV light. Thus, there is a simultaneous capture of electrons as well as holes without the interference from the complication of

transporting the low mobility holes through the oxide when the holes are generated at the oxide surface by the 10.2 eV light. Experiments performed using KeV electron beams have indicated that high densities of both oxide traps and interface states are generated. The study of generation mechanisms of oxide traps and interface states by KeV electron beam has two important applications aside from its contribution to the development of atomic models of these imperfection states. One of these is the use of electron beam to evaporate gate and interconnection metal for VLSI and VHSIC high density and high performance integrated circuits. Radiation damage will be introduced by the x-rays generated by the KeV electron beam which hits the metal target. Another is the use of electron beam to define submicron geometry. Both electron beam evaporation and electron beam lithography can produce substantial amounts of interface states and oxide traps which are detrimental to the performance of the integrated circuits.

A number of KeV electron irradiation experiments have been performed on both radiation hard and radiation sensitive MOS capacitors. After the electron beam exposure, detailed measurements of C-V, photo I-V data were taken to determine the density of interface states and oxide traps. The time dependencies of the C-V curves are also recorded as a function of radiation dose and radiation time to determine the capture rates.

Results indicated that the oxide traps have a more complicated spatial distribution than that produced by VUV light whose oxide traps are nearly all concentrated within 50A of the oxide silicon interface. A preliminary analysis of the photo I-V data showed that three superimposed

oxide charge distributions are required to explain the shapes of the photo I-V curves. One of these is a positive gaussian peak at the oxide-silicon interface with a width of 15A, similar to that produced by the VUV light. A second distribution is a nearly constant but low density of positive charge over the entire oxide. The third is a negative peak distribution about 100A from the metal-oxide (Al-SiO_2) interface with a gaussian width of 80A. Such a composite oxide charge distribution has not been reported previously. Calculation of the charge distribution profile is further complicated by the simplifying assumptions made in the theory which is used to analyze the photo I-V characteristics. A detailed analysis of the currently used photo I-V theory and a comparison of the theory with experiments has indicated that the image potential model and the static dielectric screening assumption may not be accurate or valid. This would cast considerable doubt on the accuracy or even the meaning of the charge centroid positions derived from the use of the conventional photo I-V theory to interpret experimental data. There is an intense effort in our group at this writing to resolve this problem and unfortunately the results will not be reported under the support of this research office.

IV. CUMULATIVE CHRONOLOGICAL LIST OF PUBLICATIONS

1. M.J. McNutt, J.M. Holtkamp and C.T. Sah
Differential equation solutions of MOS transmission line models
generalized to lossy cases
Solid-State Electronics, v21, 1145-1148, September 1978
2. K. Hess and C.T. Sah
Hot electrons in short-gate charge-coupled devices
IEEE Transactions on Electron Devices, vED-25, 1399-1405, December 1978
3. C.C. Shiue and C.T. Sah
New mobility-measurement technique on inverted semiconductor surfaces
near the conduction threshold
Physical Review B, v19, 2149. 2162, 15 February 1979
4. Philip C.H. Chan and C.T. Sah
Exact equivalent circuit model for steady-state characterization
of semiconductor devices with multiple-energy-level recombination
centers
IEEE Transaction on Electron Devices, vED-26, 924-936, June 1979
5. Philip C.H. Chan and C.T. Sah
Experimental and theoretical studies of I-V characteristics of
zinc-doped silicon p-n junctions using the exact DC circuit model
IEEE Transactions on Electron Devices, vED-26, 937-941, June 1979
6. Philip C.H. Chan and C.T. Sah
Computer-aided study of steady-state carrier lifetimes under arbitrary
injection conditions
Solid-State Electronics, v22, 1182-1188, December 1979
7. C.C. Shiue and C.T. Sah
Theory and experiment of electron mobility on silicon surface in
weak inversion
Proceedings of the Third International Conference on Electronic
Properties of Two-Dimensional Systems, pp. 173-178, September 3-6, 1979.
Special Issue of Surface Science, December 1979.
8. K. Hess, J.F. Detry and C.T. Sah
Trapping noise in Charge Coupled Devices
Phys. Stat. Sol. (a) 55, 243-249, 1979
9. K. Hess and C.T. Sah
The ultimate limits of CCD performance imposed by hot electron effects
Solid-State Electronics, v22, 1025-1033, 1979
10. Allen P.I. Ho and C.T. Sah
A quasi-three dimensional large-signal circuit model for lateral
transient analysis of MOS device
Solid-State Electronics, v23, 305-315, April 1980

11. A.R. Stivers and C.T. Sah
A study of the oxide traps and interface states of the silicon-silicon dioxide interface
Journal of Applied Physics, v51, 6292-6304, December 1980
12. Y. C. Sun and C. T. Sah
Interface edge effect and its contribution to the frequency dispersion of metal-oxide-semiconductor admittance
Solid State Electronics, v24, 569-576, June 1981
13. C. T. Sah, P. C. Chan, C. K. Wang. R. L-Y Sah, K. A. Yamakawa and R. Lutwack
Effect of zinc impurity on silicon solar-cell efficiency
IEEE Transaction on Electron Devices, vED-28, 304-313, March 1981

V. LIST OF PROFESSIONAL PERSONNEL

APPENDIX C
LIST OF TECHNICAL PERSONNEL

<u>Name</u>	<u>Degrees Received</u>		<u>Position</u>
*C.T. Sah			Principal Investigator
Phil C.H. Chan	M.S.E.E.	1975	Research Assistant, 1974-1978
	Ph.D.E.E.	1978	IBM Postdoctoral Fellow and Assistant Professor, EE, 1978-1981
Alan R. Stivers	M.S. Physics	1975	Research Assistant, 1974,1977,1978
	Ph.D.Physics	1979	University Fellow (Physics) 1976 Intel Corporation, Santa Clara, 1979
*James F. Detry	M.S.E.E.	1977	University Fellow (EE), 1976 Research Assistant, 1977, 1979 IBM Predoctoral Fellow (EE), 1978 Teaching Assistant, 1980-1981
*Jack Y.C. Sun	M.S.E.E.	1978	Rotary International Fellow, 1977 Research Assistant 1978-1979 IBM Predoctoral Fellow (EE), 1980
*C.K. Wang	M.S. Physics	1977	University Fellow (Physics), 1977 Research Assistant, 1978-1979 Teaching Assistant 1980 Fairchild Semiconductor 1981
Roger N. Switzer	B.S.E.E.	1977	Laboratory Assistant, 1976-1977
	M.S.E.E.	1979	University Fellow (EE), 1978-1979 Research Assistant, 1978-1979 Hewlett-Packard Co. Fort Collins, CO
*Daniel B. Jackson	B.S.E.E.	1978	Research Assistant, 1979
	Worcester Polytech.		Teaching Assistant, 1980,1981
*Joseph Tzou	M.S.E.E.	1980	
	M.S. Physics	1978	University Fellow (Physics) 1977-78 Teaching Assistant, 1979 Research Assistant, 1979,1980 Teaching Assistant, 1980,1981
*Michael A. Artaki	M.S. Physics	1979	Teaching Assistant, 1979,1980,1981
*Thomas Liu	Senior E.E.		Laboratory Assistant, 1979-1981
*Mary L. Rasmussen	Senior Computer Science		Laboratory Assistant, 1979-1981

*Continuing member

<u>Name</u>	<u>Degrees Received</u>	<u>Position</u>
Cheryl Utz	Senior, English	Laboratory Assistant, 1978-80
Sena McDaniel	Senior, English	Clerk-Typist, 1979-1980
*Donna Stowe	Senior, English	Laboratory Assistant, 1979-1981
Ming-fu Li		Visiting Scholar, 1979-1981
Guo-gang Qin		Visiting Associate Professor, 1981

*Continuing member

VI. INTERACTIONS (COUPLING ACTIVITIES)

6.1 Contract Sponsors

The principal investigator (PI) has been supported by a contract at the University of Illinois with the Rome Air Development Center at the HANSCOM AFB. He has interacted with Dr. Jerry Silverman and Dr. S. Rooslid on both this AFOSR grant and the RADC contract which concerns the performance limitations of CCD (charge coupled devices) for signal processing.

6.2 U.S. Government Laboratories

The PI has interacted with NASA and DOE Laboratories and personnel and visited their facilities on photovoltaics for space and terrestrial applications. A visit was made at the NASA Lewis Research Center with Dr. Brandhorst on August 31, 1979. The PI has attended DOE meetings on Photovoltaic Program Review in September 1979 at Denver and in November 1980 at Colorado Springs and a meeting on the high efficiency solar cell for space applications in October, 1980 where he had an extended discussion with and advised Dr. Roger Hardy of SERI (DOE) on future directions of photovoltaic power generation. The PI also served as a consultant to NASA-JPL on amorphous silicon solar cells and solar cell material manufacturing problems and has attended many project integration meetings.

6.3 U.S. Government Agencies

The PI has served for three years as the committeeman of the U.S. National Academy of Science in charge of reviewing proposals submitted to the Army Research Office in the area of electron devices. He has provided detailed written background technical information in the submircon solid state device area to Dr. Horst R. Wittmann of ARO on two recent occasions.

6.4 U.S. Government Agencies

The PI had discussed and corresponded with Dr. Jay Harris of the National Science Foundation in May, 1980 on the U.S.-China scientific exchange program, and about the NSF submicron facility on an earlier occasion.

6.5 U.S. Universities

The PI has collaborated and served as a consultant on semiconductor physics and device theory to Professors F.A. Lindholm, Jerry Fossum and Arnost Neugraoschel of the University of Florida, Gainesville. This interaction has continued for fourteen years, beginning with Lindholm and has been quite vigorous, involving contacts by mail, phone or in person on the average of twice a month.

6.6 U.S. Industries

The PI had visits or held technical discussion on solid state devices, integrated circuits and electronic materials with members of the following organizations on various occasions during 1978-1981: Control Data Corporation, Honeywell Corporation, Spire Corporation, Intel Corporation, American Micro Systems, Inc., Supertek, Fairchild Camera and Instruments Corporation, IBM, Texas Instruments, Burrough, Rockwell International, Eastman Kodak, Xerox, Westinghouse, Hewlett Packard, Hughes Aircraft, Delco, Monsanto, Gould, Tektronix.

6.7 Foreign Government - China

The PI was invited by the Chinese Academy of Science and Fudan University to visit China in April, 1980. He gave more than twenty lectures

on solar energy, photovoltaic power generation and solid state devices and physics in six key Chinese universities and three research institutes of the Chinese Academy of Science. He was also given detailed tours of several of their advanced development and engineering integrated circuit laboratories and factories.

6.8 Foreign Government - Taiwan

The PI was invited by the Taiwan National Science Council to visit Taiwan in July, 1980 and to make an in-depth evaluation of their undergraduate and graduate education programs in solid state electronics at the four national universities in Taiwan. He has also given detailed tours of their state-of-the-art silicon integrated circuit development center, which was implemented under a contract with RCA (Princeton, NJ), as well as a number of defense related engineering laboratories.

6.9 Foreign Visitors

The PI had technical visits at Urbana from Professor Karl Seeger of Solid State and Semiconductor Physics of the University of Vienna on February 19, 1978; Mr. Kinji Miyata of Hitachi (former Research Associate) on June 22, 1978; Mr. K. Wada of Fujitsu on September 26, 1978; Mr. Rod Tucker of Queensland University on October 2, 1978; Professor Hsieh Hsi-teh of Fudan University on December 10, 1979 and December 1980; Dr. H. Katto (former Research Associate) of Hitachi in December, 1980.

6.10 U.S. Professional Society

The PI served as the session chairman of the American Physical Society Meeting in Chicago on January 21, 1980. He is also the chairman of the

conference summary session of the Heavy Doping Effects Conference at the University of Florida on May 9, 1980.

